Fig. 1

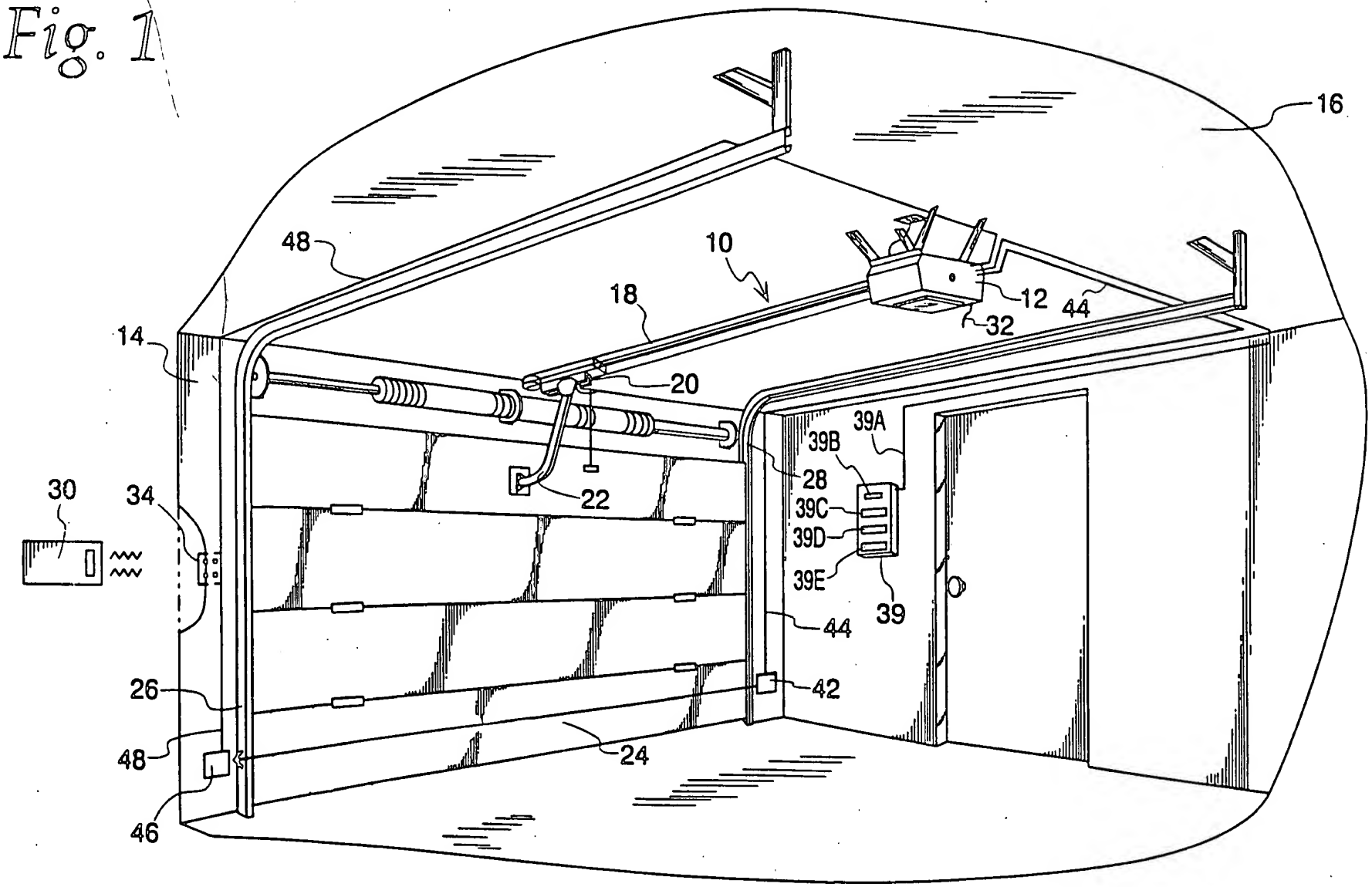
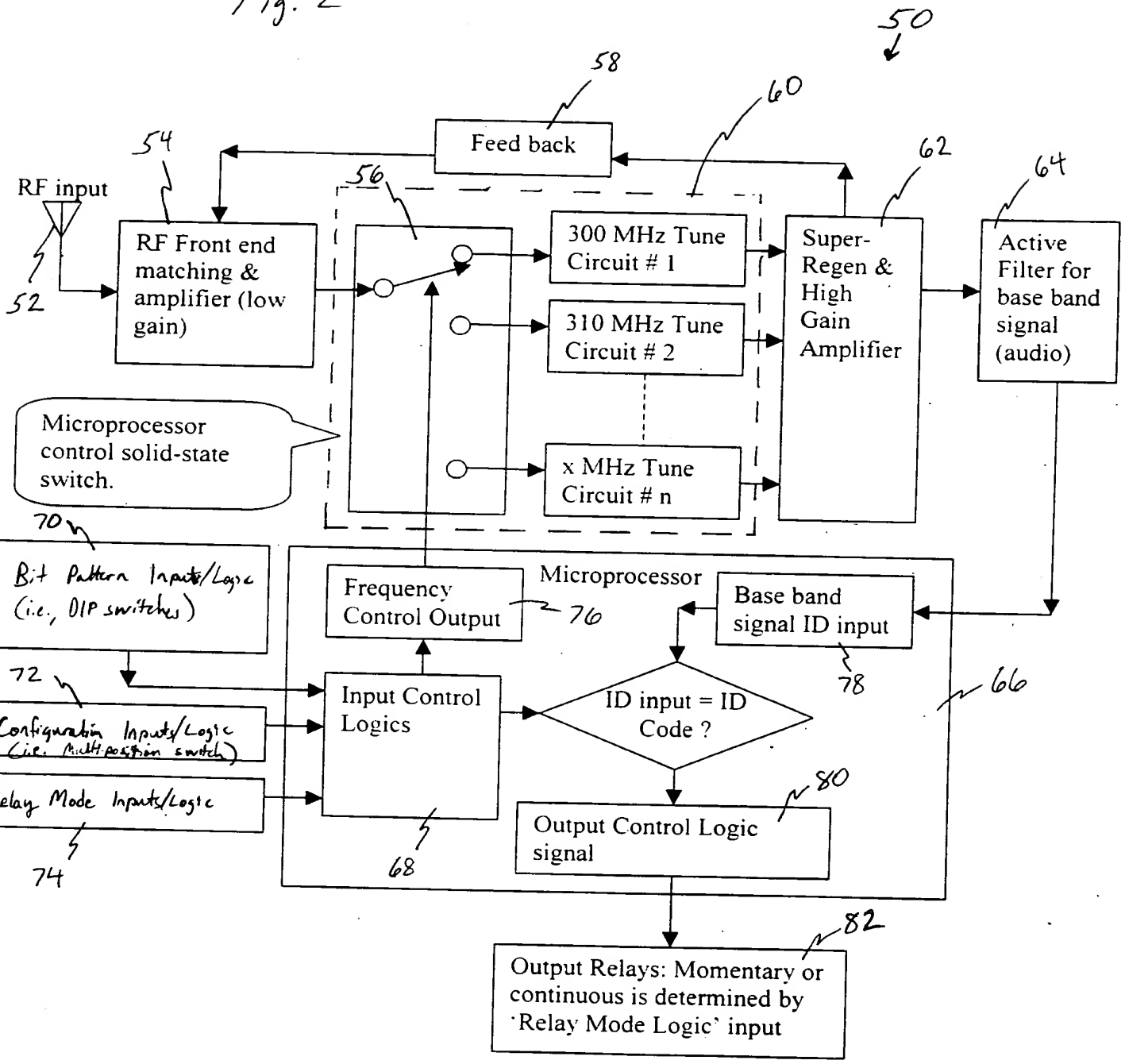


Fig. 2


50
58
Feed back
60
54
56
62
64
RF input
52
RF Front end matching & amplifier (low gain)
300 MHz Tune Circuit # 1
310 MHz Tune Circuit # 2
x MHz Tune Circuit # n
Super-Regen & High Gain Amplifier
Active Filter for base band signal (audio)
Microprocessor control solid-state switch.
70
Bit Pattern Inputs/Logic (i.e., DIP switches)
72
Configuration Inputs/Logic (i.e. Multi-position switch)
Relay Mode Inputs/Logic
74
Microprocessor
Frequency Control Output
76
Base band signal ID input
78
66
Input Control Logics
68
ID input = ID Code ?
80
Output Control Logic signal
82
Output Relays: Momentary or continuous is determined by 'Relay Mode Logic' input

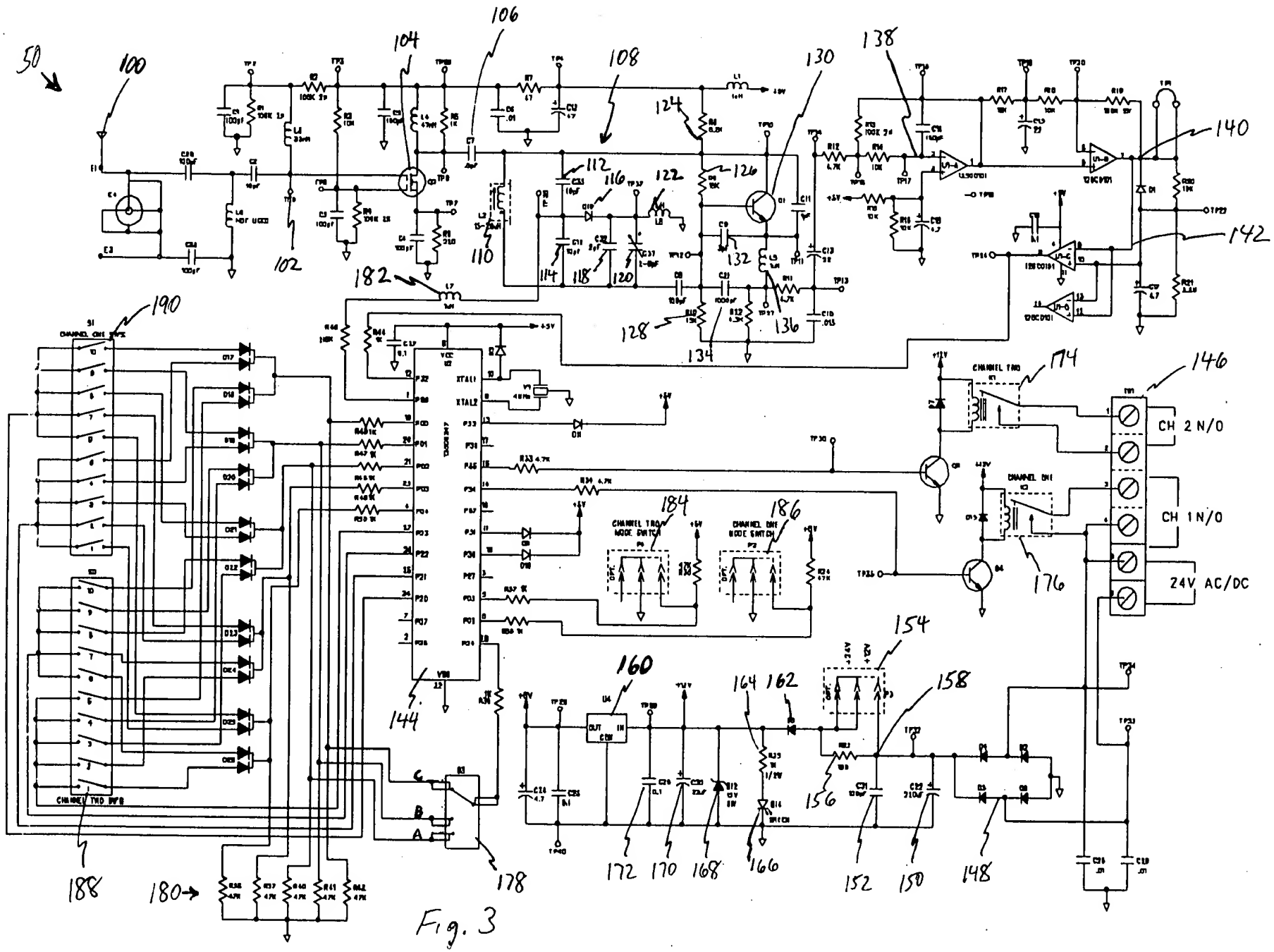


Fig. 3

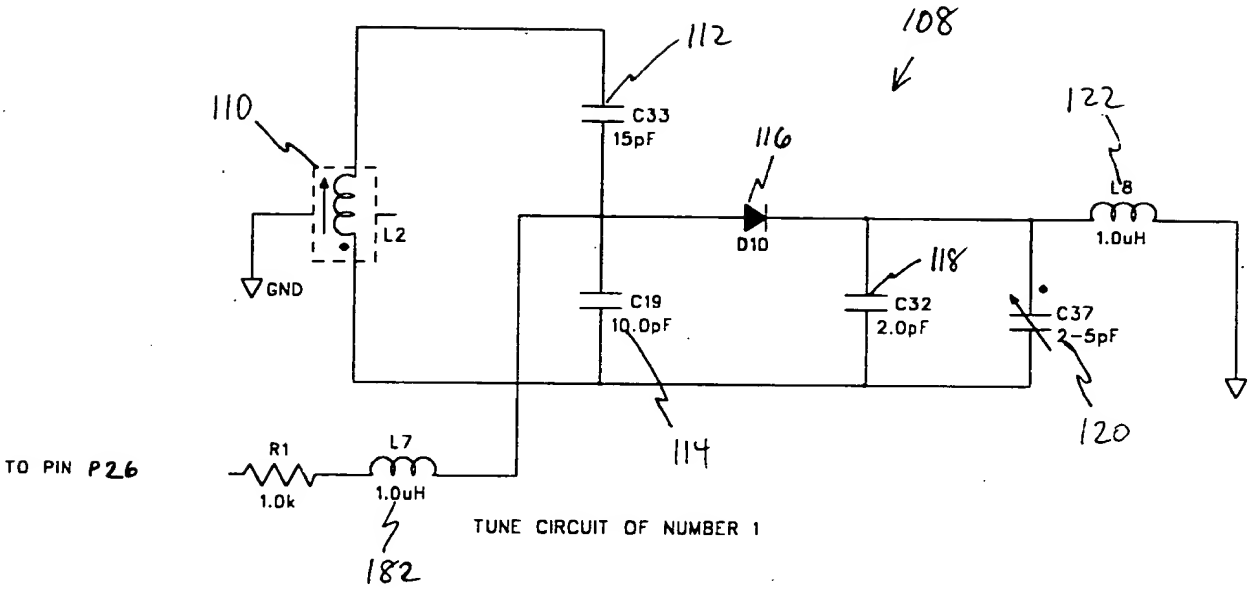

108
112
110
C33
15pF
116
122
L8
1.0uH
L2
GND
D10
118
C19
10.0pF
C32
2.0pF
C37
2-5pF
120
114
TO PIN P26
R1
1.0k
L7
1.0uH
182
TUNE CIRCUIT OF NUMBER 1

Fig. 4A

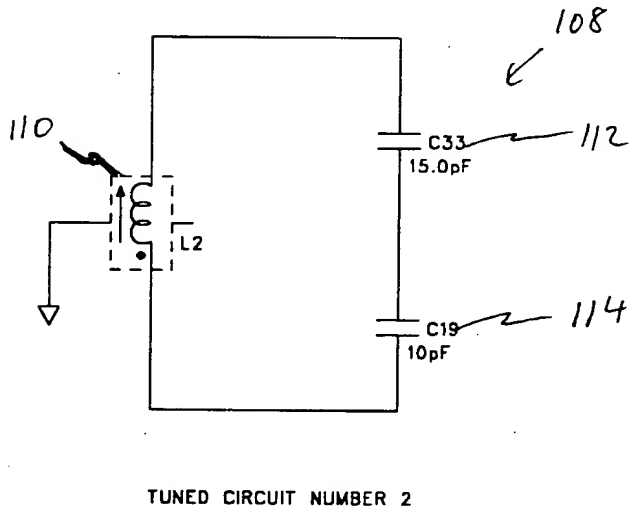

108
110
C33
15.0pF
112
L2
C19
10pF
114
TUNED CIRCUIT NUMBER 2

Fig. 4B

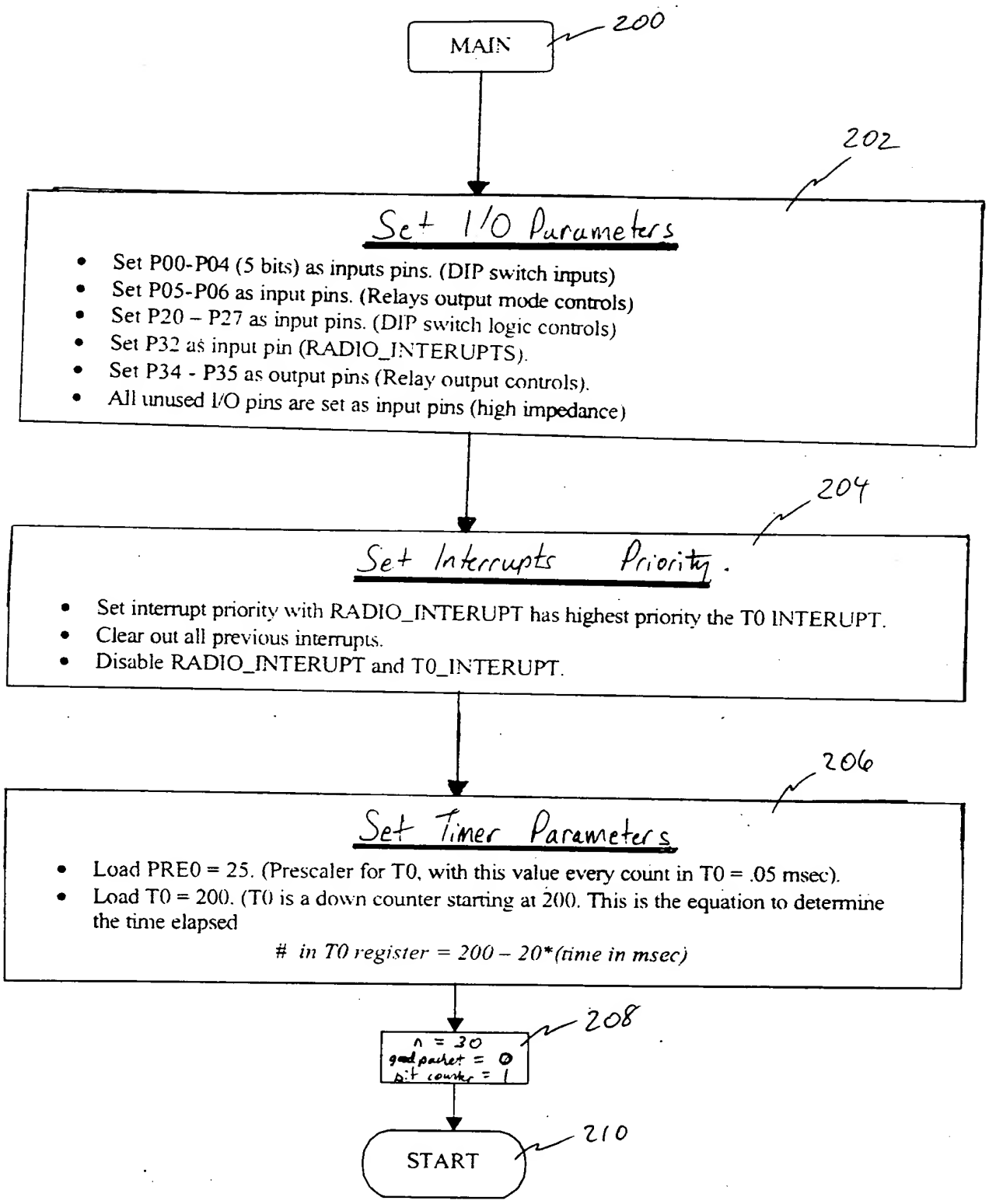

MAIN
200
202
Set I/O Parameters
• Set P00-P04 (5 bits) as inputs pins. (DIP switch inputs)
• Set P05-P06 as input pins. (Relays output mode controls)
• Set P20 – P27 as input pins. (DIP switch logic controls)
• Set P32 as input pin (RADIO_INTERUPTS).
• Set P34 - P35 as output pins (Relay output controls).
• All unused I/O pins are set as input pins (high impedance)
204
Set Interrupts Priority.
• Set interrupt priority with RADIO_INTERUPT has highest priority the T0 INTERUPT.
• Clear out all previous interrupts.
• Disable RADIO_INTERUPT and T0_INTERUPT.
206
Set Timer Parameters
• Load PRE0 = 25. (Prescaler for T0, with this value every count in T0 = .05 msec).
• Load T0 = 200. (T0 is a down counter starting at 200. This is the equation to determine the time elapsed
# in T0 register = 200 – 20*(time in msec)
n = 30
good packet = 0
bit counter = 1
208
START
210

Fig. 5A

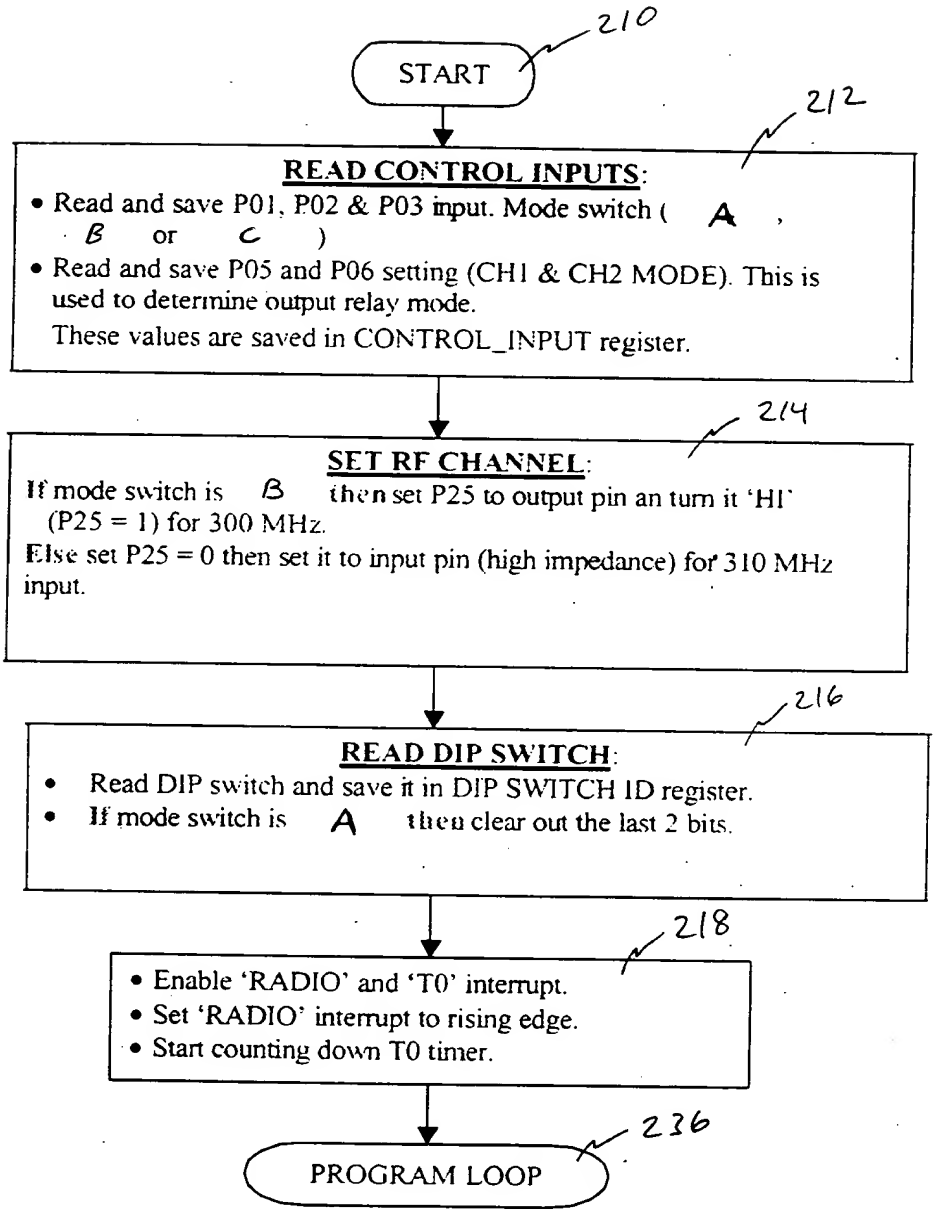

210
START
212
READ CONTROL INPUTS:
• Read and save P01, P02 & P03 input. Mode switch (A , B or C)
• Read and save P05 and P06 setting (CH1 & CH2 MODE). This is used to determine output relay mode.
These values are saved in CONTROL_INPUT register.
214
SET RF CHANNEL:
If mode switch is B then set P25 to output pin an turn it 'HI' (P25 = 1) for 300 MHz.
Else set P25 = 0 then set it to input pin (high impedance) for 310 MHz input.
216
READ DIP SWITCH:
• Read DIP switch and save it in DIP SWITCH ID register.
• If mode switch is A then clear out the last 2 bits.
218
• Enable 'RADIO' and 'T0' interrupt.
• Set 'RADIO' interrupt to rising edge.
• Start counting down T0 timer.
236
PROGRAM LOOP

Fig. 5B

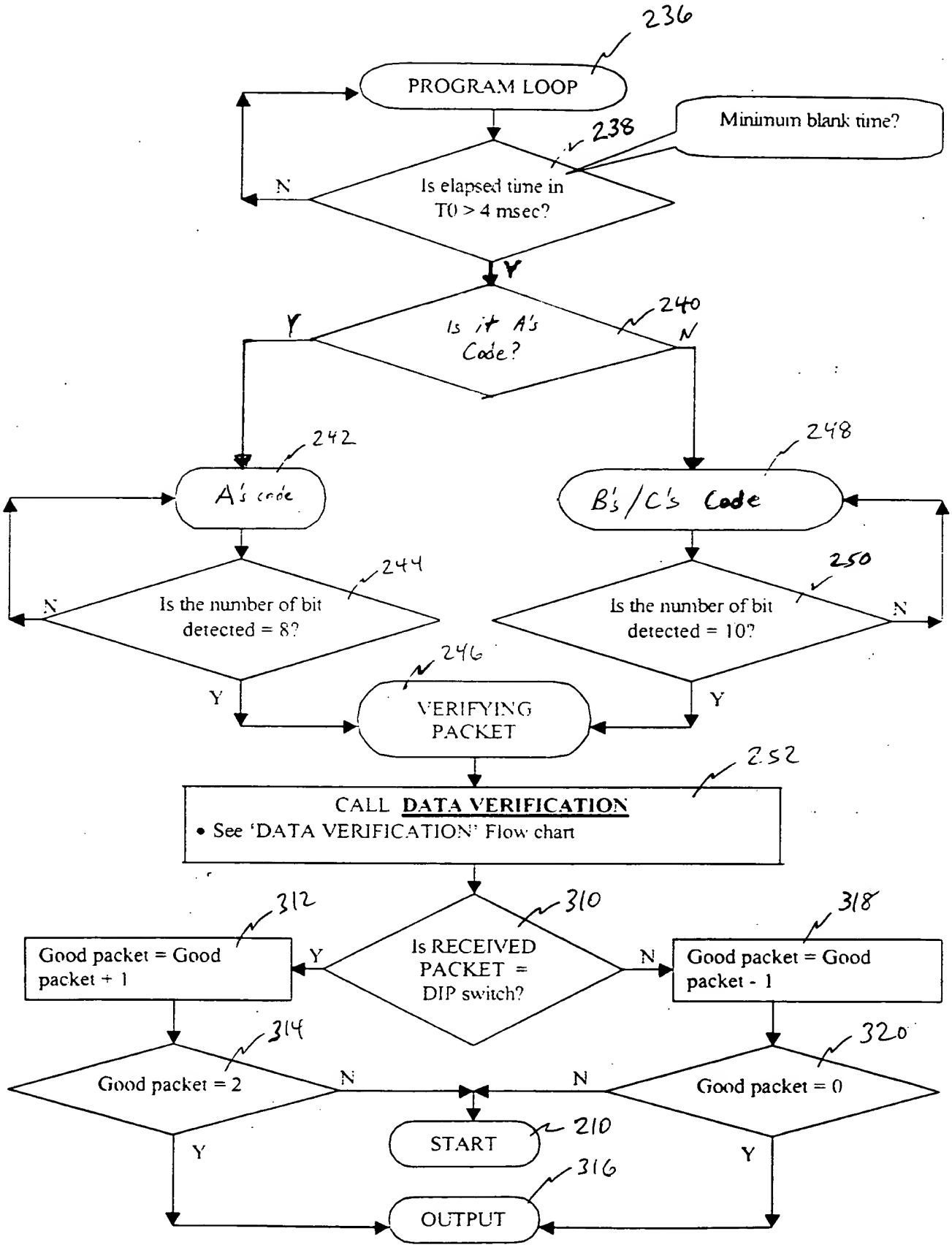

236
PROGRAM LOOP
238
Minimum blank time?
Is elapsed time in T0 > 4 msec?
N
Y
240
Is it A's Code?
Y
N
242
A's code
248
B's/C's Code
244
Is the number of bit detected = 8?
N
250
Is the number of bit detected = 10?
N
Y
Y
246
VERIFYING PACKET
252
CALL DATA VERIFICATION
• See 'DATA VERIFICATION' Flow chart
312
Good packet = Good packet + 1
310
Is RECEIVED PACKET = DIP switch?
Y
N
318
Good packet = Good packet - 1
314
Good packet = 2
N
N
320
Good packet = 0
Y
Y
210
START
316
OUTPUT

Fig. 5C

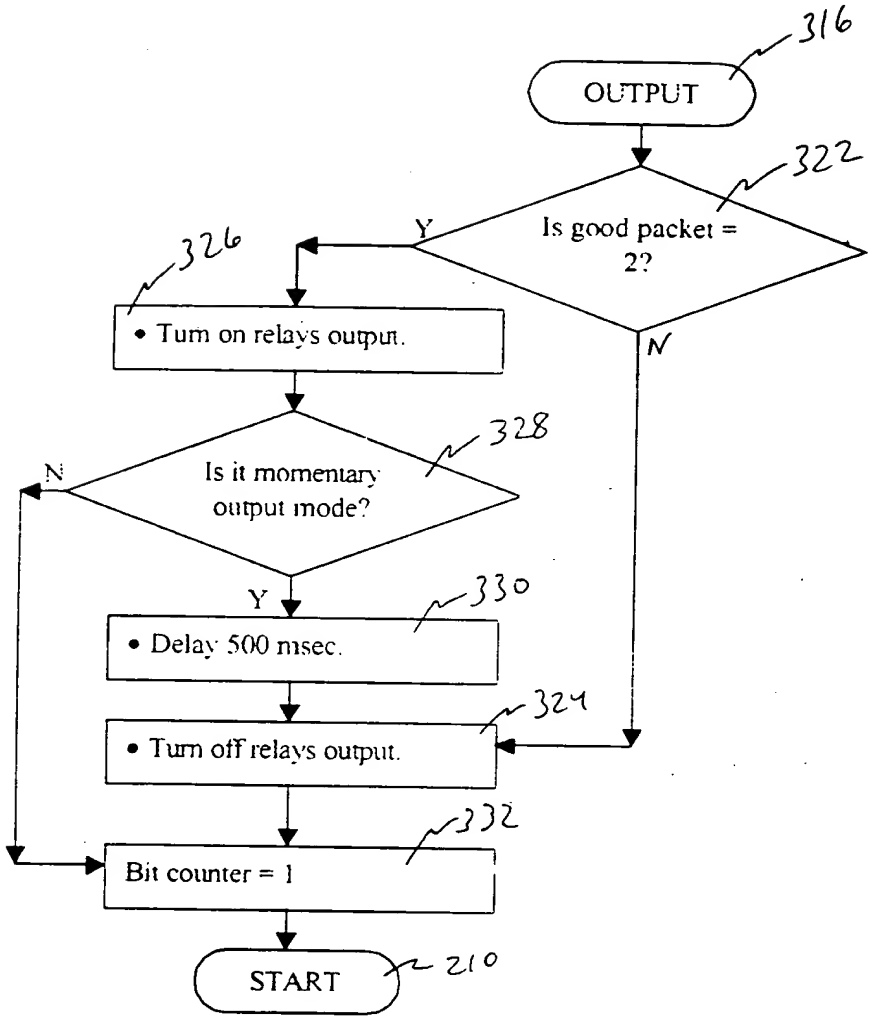

316
OUTPUT
322
Is good packet = 2?
Y
N
326
• Turn on relays output.
328
Is it momentary output mode?
N
Y
330
• Delay 500 msec.
324
• Turn off relays output.
332
Bit counter = 1
210
START

Fig. 5D

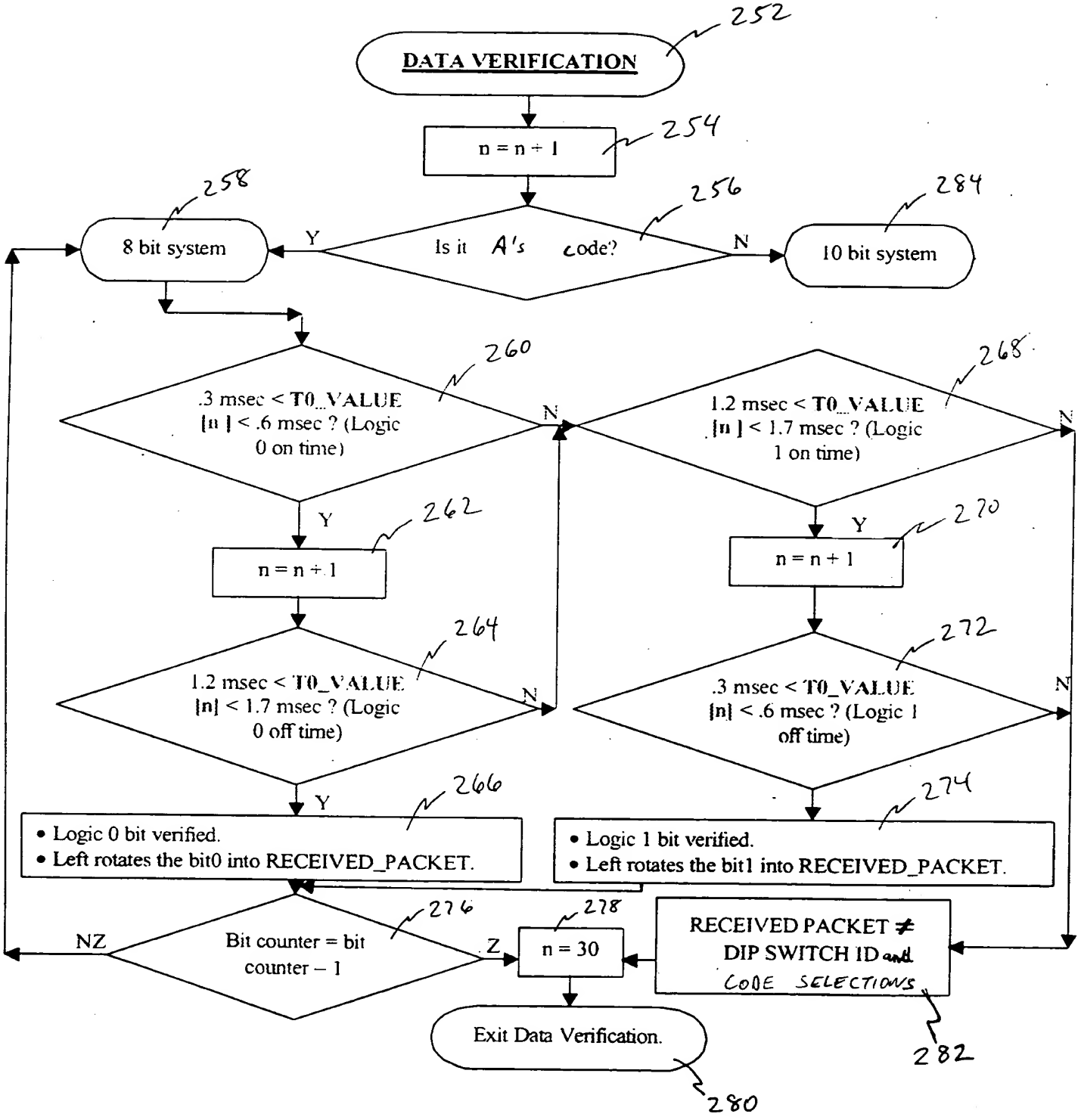

252
DATA VERIFICATION
254
n = n + 1
256
Is it A's code?
Y
N
258
8 bit system
284
10 bit system
260
.3 msec < T0_VALUE [n] < .6 msec ? (Logic 0 on time)
N
Y
262
n = n + 1
264
1.2 msec < T0_VALUE [n] < 1.7 msec ? (Logic 0 off time)
N
Y
266
• Logic 0 bit verified.
• Left rotates the bit0 into RECEIVED_PACKET.
268
1.2 msec < T0_VALUE [n] < 1.7 msec ? (Logic 1 on time)
N
Y
270
n = n + 1
272
.3 msec < T0_VALUE [n] < .6 msec ? (Logic 1 off time)
N
274
• Logic 1 bit verified.
• Left rotates the bit1 into RECEIVED_PACKET.
276
Bit counter = bit counter – 1
NZ
Z
278
n = 30
RECEIVED PACKET ≠ DIP SWITCH ID and CODE SELECTIONS
282
Exit Data Verification.
280

Fig. 5E

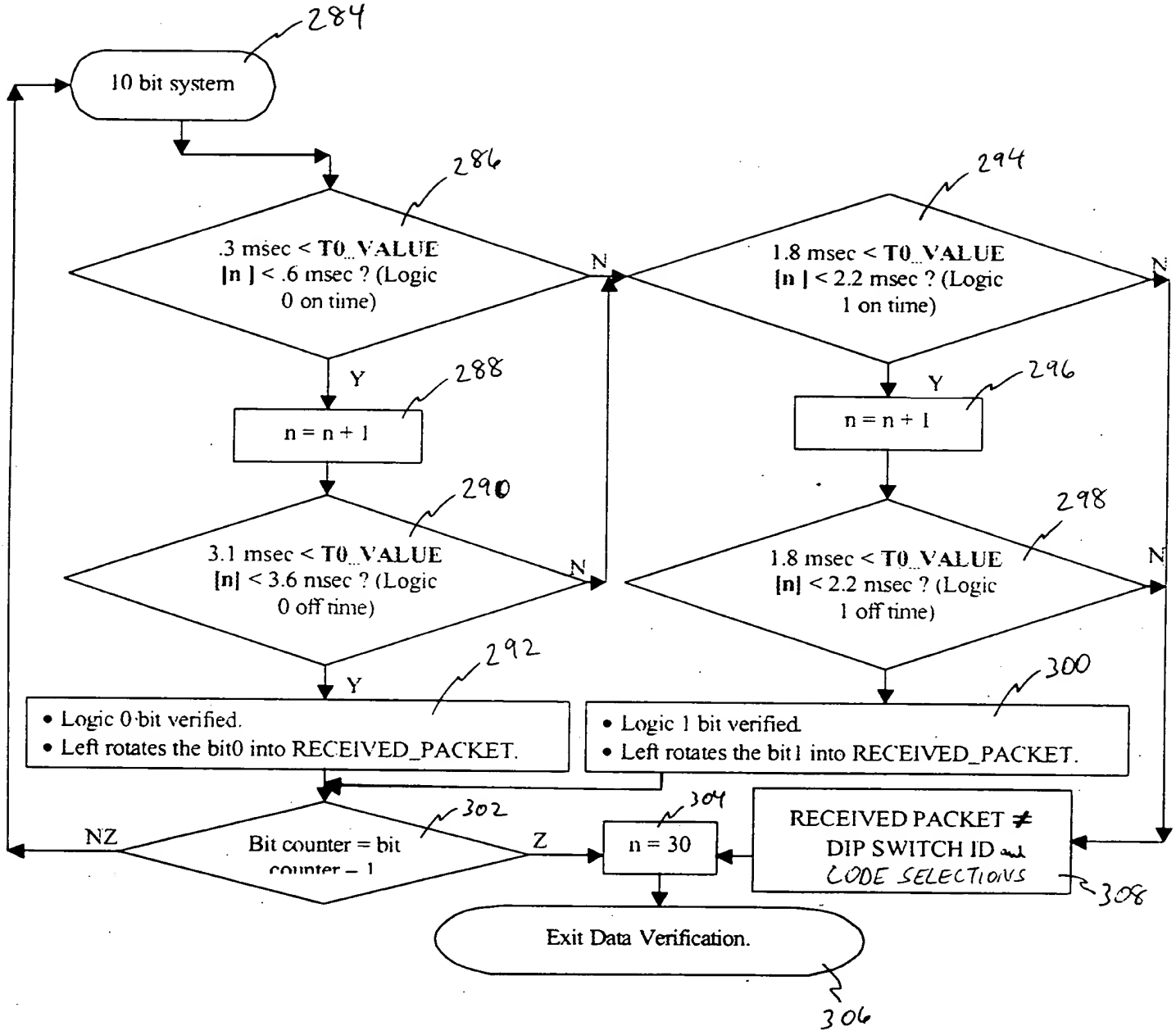

284
10 bit system
286
.3 msec < T0_VALUE |n| < .6 msec ? (Logic 0 on time)
N
Y
288
n = n + 1
290
3.1 msec < T0_VALUE |n| < 3.6 msec ? (Logic 0 off time)
N
Y
292
• Logic 0 bit verified.
• Left rotates the bit0 into RECEIVED_PACKET.
294
1.8 msec < T0_VALUE |n| < 2.2 msec ? (Logic 1 on time)
N
Y
296
n = n + 1
298
1.8 msec < T0_VALUE |n| < 2.2 msec ? (Logic 1 off time)
N
300
• Logic 1 bit verified.
• Left rotates the bit1 into RECEIVED_PACKET.
302
Bit counter = bit counter – 1
NZ
Z
304
n = 30
RECEIVED PACKET ≠ DIP SWITCH ID and CODE SELECTIONS
308
Exit Data Verification.
306

Fig. 5F

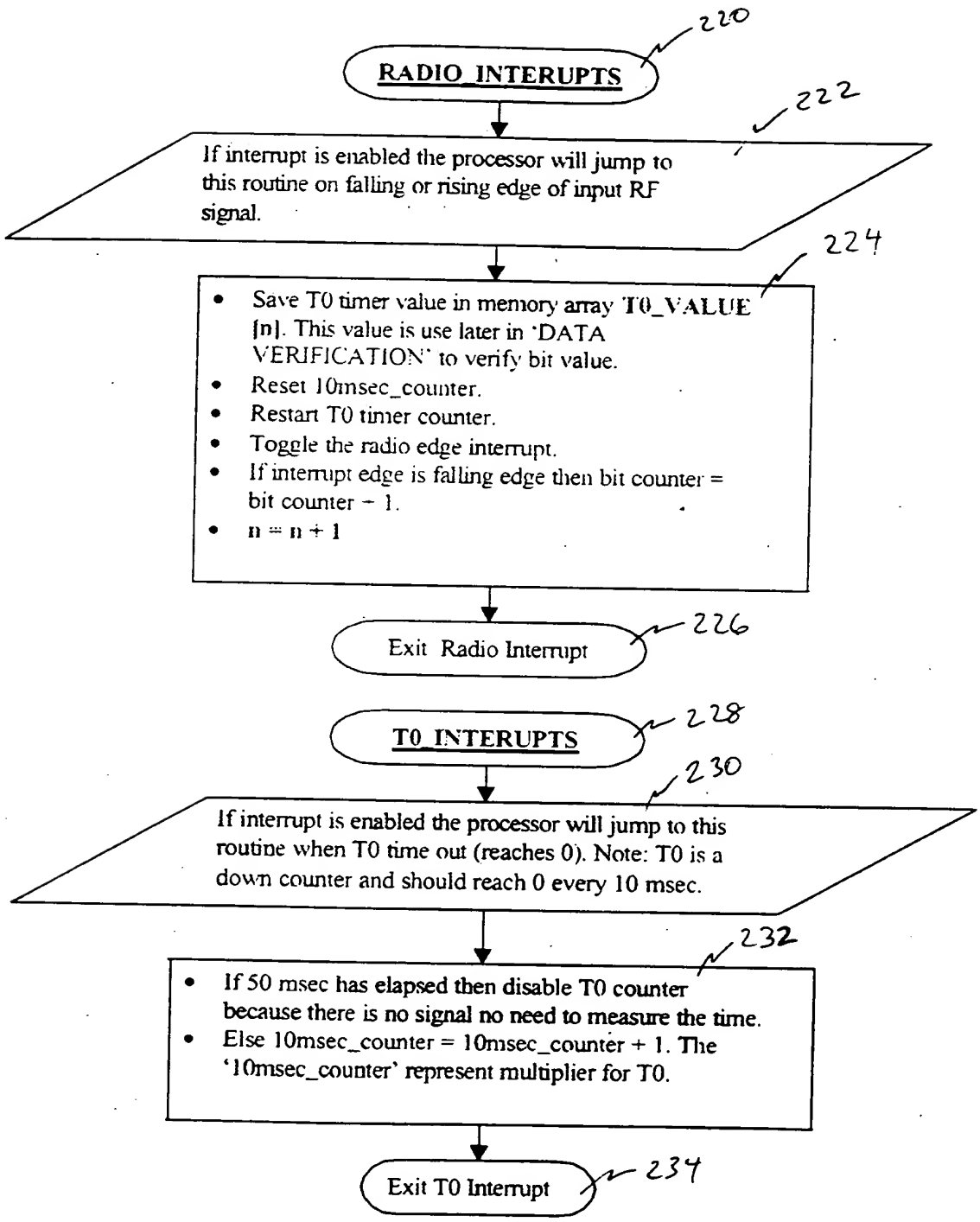

220
RADIO_INTERUPTS
222
If interrupt is enabled the processor will jump to this routine on falling or rising edge of input RF signal.
224
• Save T0 timer value in memory array T0_VALUE [n]. This value is use later in 'DATA VERIFICATION' to verify bit value.
• Reset 10msec_counter.
• Restart T0 timer counter.
• Toggle the radio edge interrupt.
• If interrupt edge is falling edge then bit counter = bit counter − 1.
• n = n + 1
226
Exit Radio Interrupt
228
T0_INTERUPTS
230
If interrupt is enabled the processor will jump to this routine when T0 time out (reaches 0). Note: T0 is a down counter and should reach 0 every 10 msec.
232
• If 50 msec has elapsed then disable T0 counter because there is no signal no need to measure the time.
• Else 10msec_counter = 10msec_counter + 1. The '10msec_counter' represent multiplier for T0.
234
Exit T0 Interrupt

Fig. 5G.